What is Claimed is:

[c1] A semiconductor chip, comprising:
a semiconductor substrate;
a rectifying contact diffusion and a non-rectifying contact diffusion in said substrate; and
a halo diffusion adjacent said rectifying contact diffusion and no halo diffusion adjacent said non-rectifying contact diffusion.

[c2] A semiconductor chip as recited in claim 1, wherein said rectifying contact is a source/drain diffusion of an FET.

[c3] A semiconductor chip as recited in claim 1, wherein said non-rectifying contact is body contact of an FET, an ohmic contact of a lateral diode, a contact of a resistor, or a contact of a capacitor.

[c4] A semiconductor chip as recited in claim 1, wherein said chip further comprises a gate conductor, wherein said rectifying contact is defined by said gate conductor.

[c5] A semiconductor chip as recited in claim 1, wherein said chip further comprises a gate conductor, wherein said non-rectifying contact is defined by said gate conductor.

[c6] A semiconductor chip as recited in claim 1, wherein said chip further comprises a gate conductor, wherein said rectifying contact and said non-rectifying contact are both defined by said gate conductor.

[c7] A semiconductor chip as recited in claim 6, wherein said rectifying contact is a source/drain diffusion of an FET and wherein said non-rectifying contact is a body contact for said FET.

[c8] A semiconductor chip as recited in claim 7, wherein said FET comprises a gate conductor, wherein said source/drain diffusions and said body contact are all defined by said gate conductor.

[c9] A semiconductor chip as recited in claim 8, wherein said FET further comprises a back insulator and a thin layer of semiconductor on said back insulator.

[c10] A semiconductor chip as recited in claim 6, wherein said rectifying contact is a diffusion of a lateral diode and wherein said non-rectifying contact is an ohmic contact to said diode.

[c11] A semiconductor chip as recited in claim 1, wherein said chip further comprises an FET comprising a source/drain diffusion and a lateral diode comprising a rectifying contact diffusion and a non-rectifying contact diffusion, wherein said rectifying contact is said source/drain diffusion of said FET and said non-rectifying contact is said non-rectifying contact diffusion of said lateral diode, and further wherein there is no halo diffusion adjacent said rectifying contact diffusion of said lateral diode.

[c12] A semiconductor chip as recited in claim 1, wherein said chip further comprises a first gate conductor and a second gate conductor, wherein said rectifying contact is defined by said first gate conductor and wherein said non-rectifying contact is defined by said second gate conductor.

[c13] A semiconductor chip as recited in claim 12, further comprising an FET and one of a lateral diode, a resistor, and a capacitor, wherein said rectifying contact is a source/drain diffusion of said FET and wherein said non-rectifying contact is an ohmic contact to said lateral diode, resistor or capacitor.

[c14] A semiconductor chip as recited in claim 13, wherein said lateral diode is for ESD protection, overshoot/undershoot protection, or over voltage clamping.

[c15] A semiconductor chip as recited in claim 13, wherein said lateral diode further comprises a rectifying contact diffusion, wherein no halo diffusion is adjacent said rectifying contact diffusion.

[c16] A semiconductor chip as recited in claim 1, further comprising a second non-rectifying contact, wherein no halo diffusion is adjacent either of said non-rectifying contacts.

[c17] A semiconductor chip as recited in claim 1, wherein the chip comprises silicon-on-insulator.

[c18] A semiconductor chip as recited in claim 1, wherein an extension diffusion is adjacent said source drain diffusion and wherein no extension diffusion is adjacent said non-rectifying contact.

[c19] A method of fabricating a semiconductor chip, comprising the steps of:
providing a semiconductor substrate;
forming a rectifying diffusion contact in said substrate;

forming a non-rectifying diffusion contact in said substrate; and
forming a halo diffusion adjacent said rectifying diffusion contact and forming no halo diffusion adjacent said non-rectifying diffusion contact.

[c20] A method as recited in claim 19, wherein in said forming step (b) said rectifying diffusion is a source/drain diffusion of an FET, wherein in said forming step (c) said non-rectifying contact is a body contact for said FET.

[c21] A method as recited in claim 19, wherein said non-rectifying diffusion contact is an electrode of a lateral diode.

[c22] A method as recited in claim 21, wherein said lateral diode is for ESD protection, overshoot/undershoot protection, or over voltage clamping.

[c23] A method as recited in claim 21, wherein in said forming step (b) said rectifying diffusion is a source/drain diffusion of an FET or a second electrode of said lateral diode.

[c24] A method as recited in claim 19, wherein in said forming step (b) said rectifying diffusion is a source/drain diffusion of an FET, wherein said forming step (c) comprises forming a device having a pair of said non-rectifying diffusion contacts and wherein said step (d) comprises forming no halo diffusion adjacent either of said non-rectifying contacts.

[c25] A method as recited in claim 24, wherein said device comprises a resistor or a capacitor.

[c26] A method as recited in claim 19, wherein in said forming step (a) said substrate comprises SOI.

[c27] A method as recited in claim 19, further comprising forming an extension diffusion adjacent said rectifying contact diffusion and forming no extension diffusion adjacent said non-rectifying contact diffusion .

[c28] A method as recited in claim 19, wherein said forming step (d) comprises providing a first mask including a location of a non-rectifying diffusion contact, wherein said first mask has a blocking region over said location.

[c29] A method as recited in claim 28, wherein said non-rectifying diffusion contact is defined by data on at least one other mask, and wherein said blocking region on said first mask is generated from said data.

[c30] A method as recited in claim 29, wherein said blocking region on said first mask is generated from said data by logically combining shapes from a plurality of masks and adjusting the result to avoid sublithographic features.